

1. A method for automatic design of a processor datapath from an input specification including a register file specification, a set of specified processor operations and a desired instruction level parallelism among the specified operations, the method comprising:

programmatically assigning instances of functional units from a macrocell library to the sets of mutually exclusive operations, such that each specified operation is associated with a corresponding functional unit;

programmatically synthesizing register files with the allocated read/write ports and interconnects between the functional units and the allocated read/write ports.

2. The method of claim 1 wherein the ports of the functional units each have a corresponding register file port request and programmatically determining the resource allocation includes:

programmatically allocating a minimum number of read/write ports that satisfies all of the port requests.

3. The method of claim 1 wherein the specification of parallelism among operations is specified as exclusion relationships among operations that indicate which operations cannot be executed concurrently.

4. The method of claim 3 wherein the input specification further includes:

- 5 a mapping between the specified operations and register file types in the register file specification; and  
operation formats describing inputs and outputs of the specified operations.

- 10 5. The method of claim 1 wherein the synthesized functional units include macrocell instances, the synthesized register files include register file instances, and the interconnect includes macrocell instances of wires, buses, muxes, or tri-states.

- 15 6. The method of claim 1 wherein determining sets of mutually exclusive operations includes:  
finding maximal cliques of mutually exclusive operations based on exclusion relations derived from the input specification.

- 20 7. The method of claim 1 wherein synthesizing functional units includes:

building a list of valid functional units based on opcodes and latency of the specified operations;

- 25 from the list, selecting functional units such that each functional unit covers a maximum number of operations in a set of mutually exclusive operations.

8. The method of claim 1 including:

using the instruction level parallelism from the input specification to identify which functional unit ports can be allocated to the same

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9. A computer readable medium having software for performing  
5 the method of claim 1.

from an input specification defining a set of specified processor  
10 operations and instruction level parallelism among the specified  
operations, determining sets of mutually exclusive operations;

15 unit; and  
programmatically synthesizing the functional units from the  
macrocell library such that the functional units are described in a  
hardware description language.

20 11. The method of claim 10 wherein determining sets of mutually exclusive operations includes:  
finding exclusion cliques where each clique represents a maximal set of mutually exclusive operations; and  
wherein assigning instances of functional units includes  
25 programmatically selecting instances of functional units to cover the cliques from the macrocell library.

building a list of valid functional units based on opcodes of the specified operations;

13. The method of claim 10 wherein functional unit instances are assigned such that the semiconductor area covered by functional units in the processor design is minimized.

15. A computer readable medium having software for performing the method of claim 10.

25 the method comprising:

for each type of register file specified in the processor,

establishing a set of read/write port requests between the functional

units and each of the register file types;

programmatically computing a resource allocation of register ports

30 in the register file types to read/write port requests, including

determining how to share a register port for two or more functional unit ports based on the specification of instruction level parallelism among the operations; and

~~programmatically synthesizing register files with the allocated read/write ports and interconnects between the functional units and the allocated read/write ports.~~

~~17. The method of claim 16 wherein the resource allocation uses a contiguous allocation heuristic that simplifies interconnect layout by allocating register port requests from a functional unit to contiguous register ports.~~

18. A computer readable medium having software for performing the method of claim 16.

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